■ Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.
- The charger section can be connected up to absolute maximum rating 24V.

② Detection voltage precision
- Overcharge detection voltage

±60mV (Ta=25℃)

- Overdischarge detection voltage

±110mV (Ta=25℃)

- Discharging overcurrent detection voltage

±35mV (Ta=25℃)

③ Built-in detection delay times
- Overcharge detection delay time

Min 0.001s / Typ 0.08s / Max 0.20s (Ta=25℃)

- Overdischarge detection delay time)

Min 1ms / Typ 40ms / Max 100ms (Ta=25℃)

- Discharging overcurrent detection delay time)

Min 1ms / Typ 10ms / Max 30ms (Ta=25℃)

- Short detection delay time)

Typ 300μs / Max 800μs (Ta=25℃)

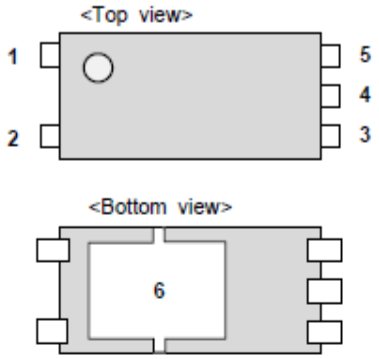
④ With abnormal charger detection function
⑤ 0V charge function is allowed
⑥ Auto Wake-up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.
② Common drain configuration
③ General characteristics
- V_{DS} (V) = 20V
- I_D (A) = 6A
- $R_{SS(ON)}$ < 60mΩ (V_{GS} = 4.5V, I_D = 1A)

■ Pin Assignment

[Package: TEP-5L]



1	TP (N.C)
2	Source 1(same as VSS)
3	Source 2
4	VDD
5	V-
6	Drain

■ Block Diagram