Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process

- The charger section can be connected up to absolute maximum rating 26V.

② Detection voltage precision

- Overcharge detection voltage

±35㎷ (Ta=25℃), ±55㎷ (Ta=-30~70℃)

- Overdischarge detection voltage

±100㎷ (Ta=25℃), ±110㎷ (Ta=-30~70℃)

- Discharge overcurrent detection voltage

±25㎷ (Ta=25℃), ±40㎷ (Ta=-30~70℃)

- Charging overcurrent detection voltage

±35㎷ (Ta=25℃), ±50㎷ (Ta=-30~70℃)

③ Built-in detection delay times (timer circuit)

- Overcharge detection delay time

1.00±0.4s(Ta=25℃), 1.00[+0.7, −0.6]s (Ta=-30~70℃)

- Overdischarge detection delay time

77.0±63㎳ (Ta=25℃), 77.0[+93.0, −64.2]㎳ (Ta=-30~70℃)

- Discharge overcurrent detection delay time

13.0±9.0㎳ (Ta=25℃), 13.0[+15.9, −10.5]㎳ (Ta=-30~70℃)

- Charging overcurrent detection delay time

20.0±15.0㎳ (Ta=25℃), 20.0[+20.0, −15.6]㎳ (Ta=-30~70℃)

- Short detection delay time

700[+600, −587.5]㎲ (Ta=25℃), 700[+1050, −602]㎲ (Ta=-30~70℃)

④ 0V charge function is allowed

⑤ Auto Wake-up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

② The protection for ESD

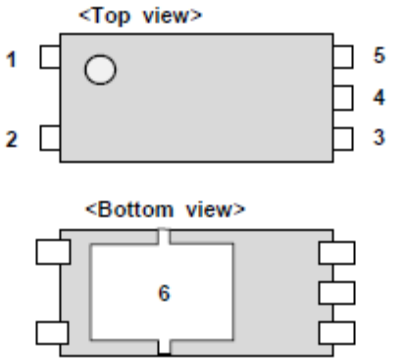
③ Common drain configuration

④ General characteristics

- V_{DS} (V) = 20V
- I_D (A) = 6A
- $R_{DS(ON)}$ < 50mΩ (V_{GS} = 4.5V, I_D = 5A)
- ESD Rating : 2000V HBM

Pin Assignment

[Package: TEP-5L]



1	N.C
2	Source 1(same as V_{SS})
3	Source 2
4	V_{DD}
5	V−
6	Drain

Block Diagram