

■ Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

- ① Uses high withstand voltage CMOS process
 - The charger section can be connected up to absolute maximum rating 28V.
- ② Detection voltage precision
 - Overcharge detection voltage $\pm 25mV$ ($T_a=25^\circ C$), $\pm 45mV$ ($T_a=-30\sim 76^\circ C$)
 - Overdischarge detection voltage $\pm 35mV$ ($T_a=25^\circ C$), $\pm 75mV$ ($T_a=-30\sim 76^\circ C$)
 - Discharge overcurrent detection voltage $\pm 10mV$ ($T_a=25^\circ C$), $\pm 20mV$ ($T_a=-30\sim 76^\circ C$)
- ③ Built-in detection delay times (timer circuit)
 - Overcharge detection delay time $6.25 \pm 1.25s$ ($T_a=25^\circ C$), $6.25[+3.13, -2.5]s$ ($T_a=-30\sim 76^\circ C$)
 - Overdischarge detection delay time $96.0 \pm 19.2ms$ ($T_a=25^\circ C$), $96.0[+48, -38.4]ms$ ($T_a=-30\sim 76^\circ C$)
 - Discharge overcurrent detection delay time $12.0 \pm 2.4ms$ ($T_a=25^\circ C$), $12.0[+6, -4.8]ms$ ($T_a=-30\sim 76^\circ C$)
 - Short detection delay time $400[+160, -120]\mu s$ ($T_a=25^\circ C$), $400[+400, -200]\mu s$ ($T_a=-30\sim 76^\circ C$)

- ④ With abnormal charger detection function
- ⑤ 0V charge function is allowed
- ⑥ Auto Wake-up function is not allowed

2) FET

- ① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.
- ② The protection for ESD
- ③ Common drain configuration
- ④ General characteristics
 - V_{GS} (V) = 30V
 - I_b (A) = 8A
 - $R_{DS(ON)} < 46m\Omega$ ($V_{GS} = 4.5V$, $I_b = 5A$), ($R_{DS(ON)} < 23m\Omega$)
 - ESD Rating : 2000V HBM

■ Pin Assignment

TEP-5L
<TOP VIEW>



1	V _{DD}
2	Source 1(same as V _{SS})
3	Source 2
4	N.C
5	V ₋

■ Block Diagram

