■ Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process

- The charger section can be connected up to absolute maximum rating 28V.

② Detection voltage precision

- Overcharge detection voltage

±25mV (Ta=25℃), ±45mV (Ta=-30~76℃)

- Overdischarge detection voltage

±35mV (Ta=25℃), ±75mV (Ta=-30~76℃)

- Discharge overcurrent detection voltage

±10mV (Ta=25℃), ±20mV (Ta=-30~76℃)

③ Built-in detection delay times (timer circuit)

- Overcharge detection delay time

6.25±1.25s (Ta=25℃), 6.25[+3.13, −2.5]s (Ta=-30~76℃)

- Overdischarge detection delay time

96.0±19.2ms (Ta=25℃), 96.0[+48, −38.4]ms (Ta=-30~76℃)

- Discharge overcurrent detection delay time

12.0±2.4ms (Ta=25℃), 12.0[+6, −4.8]ms (Ta=-30~76℃)

- Short detection delay time

400[+160, −120]μs (Ta=25℃), 400[+400, −200]μs (Ta=-30~76℃)

④ With abnormal charger detection function

⑤ 0V charge function is allowed

⑥ Auto Wake-up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

② The protection for ESD

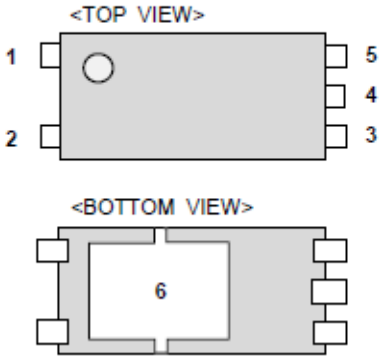
③ Common drain configuration

④ General characteristics

- V_{DS} (V) = 30V
- I_D (A) = 8A
- $R_{SS(ON)}$ < 37mΩ (V_{GS} = 3.9V, I_D = 5A)
- ESD Rating : 2000V HBM

■ Pin Assignment

[Package: TEP-5L]



1	V_{DD}
2	Source 1(same as V_{SS})
3	Source 2
4	N.C
5	V-

■ Block Diagram