■ Features

1. The protection IC and The Dual- Nch MOSFET to use common Drain are integrated into One- packaging IC.
2. Reduced Pin- Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.
- The charger section can be connected up to absolute maximum rating 30V.

② Detection voltage precision
- Overcharge detection voltage

±35㎷ (Ta=25℃), [+44, - 50]㎷ (Ta=- 30~76℃)
- Overdischarge detection voltage

±58㎷ (Ta=25℃), [+63, - 76]㎷ (Ta=- 30~76℃)
- Discharge overcurrent detection voltage

±20㎷ (Ta=25℃), [+21, - 22]㎷ (Ta=- 30~76℃)
- Charging overcurrent detection voltage

±30㎷ (Ta=25℃), ±32㎷ (Ta=- 30~76℃)

③ Built- in detection delay times (timer circuit)
- Overcharge detection delay time

5.00± 1.50s (Ta=25℃), 5.00[+3.1, −1.85] s (Ta=- 30~76℃)
- Overdischarge detection delay time

20.0± 6.0㎳ (Ta=25℃), 20.0[+12.4, −7.2]㎳ (Ta=- 30~76℃)
- Discharge overcurrent detection delay time

12.0± 4.0㎳ (Ta=25℃), 12.0[+7.4, −4.6]㎳ (Ta=- 30~76℃)
- Charging overcurrent detection delay time

16.0± 5.0㎳ (Ta=25℃), 16.0[+10.0, −6.1]㎳ (Ta=- 30~76℃)
- Short detection delay time

300[+200, −70]㎲ (Ta=25℃), 300[+295, −85]㎲ (Ta=- 30~76℃)

④ 0V charge function is allowed

⑤ Auto Wake- up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

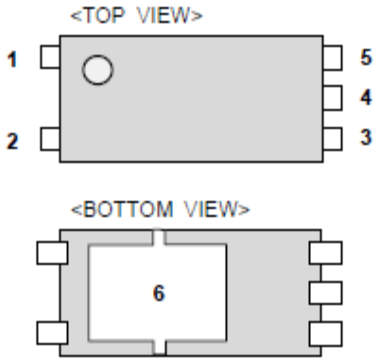
② The protection for ESD

③ Common drain configuration

④ General characteristics
- V_{DS} (V) = 24V
- I_D (A) = 7A
- $R_{DS(ON)}$ < 45mΩ (V_{GS} = 4.5V, I_D = 5A)
- ESD Rating : 2000V HBM

■ Pin Assignment

[Package: TEP-5L]



1	V_{DD}
2	**Source 1** (same as V_{SS})
3	**Source 2**
4	**N.C** (No connected)
5	**V-**
6	**Drain**

■ Block Diagram