

## Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.

2. Reduced Pin-Count by fully connecting internally.

3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.

- The charger section can be connected up to absolute maximum rating 28V.

② Detection voltage precision

- Overcharge detection voltage

$$\pm 25\text{mV} \text{ (Ta=25}^\circ\text{C)}, \pm 45\text{mV} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Overdischarge detection voltage

$$\pm 70\text{mV} \text{ (Ta=25}^\circ\text{C)}, \pm 80\text{mV} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Discharging overcurrent detection voltage

$$\pm 10\text{mV} \text{ (Ta=25}^\circ\text{C)}, \pm 20\text{mV} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Charging overcurrent detection voltage

$$\pm 20\text{mV} \text{ (Ta=25}^\circ\text{C)}, \pm 40\text{mV} \text{ (Ta=-30~70}^\circ\text{C)}$$

③ Built-in detection delay times

- Overcharge detection delay time

$$1.00 \pm 0.20\text{s} \text{ (Ta=25}^\circ\text{C)}, 1.00[+0.50, -0.40]\text{s} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Overdischarge detection delay time

$$96.0 \pm 19.2\text{ms} \text{ (Ta=25}^\circ\text{C)}, 96.0[+48, -38.4]\text{ms} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Discharging overcurrent detection delay time

$$12.0 \pm 2.4\text{ms} \text{ (Ta=25}^\circ\text{C)}, 12.0[+6.0, -4.8]\text{ms} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Charging overcurrent detection delay time

$$6.0 \pm 1.2\text{ms} \text{ (Ta=25}^\circ\text{C)}, 6.0[+3.0, -2.4]\text{ms} \text{ (Ta=-30~70}^\circ\text{C)}$$

- Short detection delay time

$$400[+160, -120]\mu\text{s} \text{ (Ta=25}^\circ\text{C)}, 400[+400, -200]\mu\text{s} \text{ (Ta=-30~70}^\circ\text{C)}$$

④ 0V charge function is allowed

⑤ With abnormal charger detection function

⑥ Auto Wake-up function is allowed

2) FET

① Using advanced trench technology to provide excellent  $R_{DS(on)}$ , low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V  $V_{GS(MAX)}$ .

② The protection for ESD

③ Common drain configuration

④ General characteristics

-  $V_{DS}$  (V) = 24V

-  $I_D$  (A) = 7A

-  $R_{DS(on)} < 48\text{m}\Omega$  ( $V_{GS} = 3.9\text{V}$ ,  $I_D = 5\text{A}$ )

- ESD Rating : 2000V HBM

## Pin Assianment

[ Package: TEP-5L ]

<Top view>



<Bottom view>



1	N.C
2	Source 1(same as V <sub>SS</sub> )
3	Source 2
4	V <sub>DD</sub>
5	V <sub>-</sub>
6	Drain

## Block Diagram

