Features

1. The protection IC and The Dual-Nch **MOSFET to use common Drain are integrated into** One-packaging IC.
2. Reduced Pin-Count by fully connecting **internally.**
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS **process.**
- The charger section can be **connected up to absolute maximum rating 28V.**

② Detection voltage precision
- Overcharge detection voltage

±25mV (Ta=25℃), ±45mV (Ta=-30~70℃)
- Overdischarge detection voltage

±70mV (Ta=25℃), ±80mV (Ta=-30~70℃)
- Discharging overcurrent detection **voltage**

±10mV (Ta=25℃), ±20mV (Ta=-30~70℃)
- Charging overcurrent detection **voltage**

±20mV (Ta=25℃), ±40mV (Ta=-30~70℃)

③ Built-in detection delay times
- Overcharge detection delay time

1.00±0.20s (Ta=25℃), 1.00[+0.50, −0.40]s (Ta=-30~70℃)
- Overdischarge detection delay **time)**

20.0±4.0ms (Ta=25℃), 20.0[+10.0, −8.0]ms (Ta=-30~70℃)
- Discharging overcurrent detection **delay time)**

12.0±2.4ms (Ta=25℃), 12.0[+6, −4.8]ms (Ta=-30~70℃)
- Charging overcurrent detection **delay time)**

16.0±3.2ms (Ta=25℃), 16.0[+8.0, −6.4]ms (Ta=-30~70℃)
- Short detection delay time)

400[+160, −120]μs (Ta=25℃), 400[+400, −200]μs (Ta=-30~70℃)

④ With abnormal charger has an **ability to detect function**

⑤ 0V charge function is allowed

⑥ **Auto Wake-up function is allowed**

2) FET

① **Using advanced trench technology to provide** excellent $R_{DS(ON)}$, low gate charge and **operation with gate voltage as low as** 2.5V while retaining a 12V $V_{GS(MAX)}$.

② **The protection for ESD**

③ **Common drain configuration**

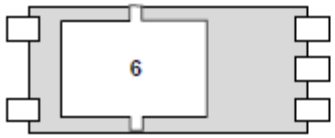
④ **General characteristics**
- V_{DS} (V) = 24V
- I_D (A) = 7A
- $R_{SS(ON)}$ < 46mΩ (V_{GS} = 4.5V, I_D = 1A)
- ESD Rating : 2000V HBM

Pin Assignment

[Package : TEP-5L]

<Top view>

<Bottom view>



1	N.C
2	Source 1(same as V_{SS})
3	Source 2
4	V_{DD}
5	V−
6	Drain

Block Diagram