Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.
- The charger section can be connected up to absolute maximum rating 28V.

② Detection voltage precision
- Overcharge detection voltage

±25㎷ (Ta=25℃), ±30㎷ (Ta=-20~60℃)
- Overdischarge detection voltage

±35㎷ (Ta=25℃), ±40㎷ (Ta=-20~60℃)
- Discharging overcurrent detection voltage

±10㎷ (Ta=25℃), ±15㎷ (Ta=-20~60℃)
- Charging overcurrent detection voltage

±20㎷ (Ta=25℃), ±30㎷ (Ta=-20~60℃)

③ Built-in detection delay times
- Overcharge detection delay time

1.00±0.20s (Ta=25℃), 1.00[+0.4, -0.35]s (Ta=-20~60℃)
- Overdischarge detection delay time

20.0±4.0㎳ (Ta=25℃), 20.0[+8, -7]㎳ (Ta=-20~60℃)
- Discharging overcurrent detection delay time

12.0±3.6㎳ (Ta=25℃), 6.0[+4.8, -4.2]㎳ (Ta=-20~60℃)
- Charging overcurrent detection delay time

6.0±1.8㎳ (Ta=25℃), 8.0[+2.4, -2.1]㎳ (Ta=-20~60℃)
- Short detection delay time

400[+160, -120]㎲ (Ta=25℃), 400[+300, -175]㎲ (Ta=-20~60℃)

④ 0V charge function is not allowed

⑤ Auto Wake-up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

② The protection for ESD

③ Common drain configuration

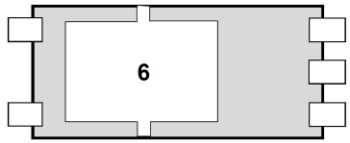
④ General characteristics
- V_{DS} (V) = 24V
- I_D (A) = 6A
- $R_{SS(ON)}$ < 47mΩ (V_{GS} = 3.7V, I_D = 4A)
- ESD Rating : 2000V HBM

Pin Assignment

[Package: TEP-5L]

<Top view>

<Bottom view>



1	**N.C**
2	**Source 1**(same as V_{SS})
3	**Source 2**
4	**V_{DD}**
5	**V–**
6	**Drain**

Block Diagram